An improved address translation method and mechanism for memory management in a computer system is disclosed. [A segmentation mechanism employing segment registers maps virtual addresses into a linear address space. A paging mechanism optionally maps linear addresses into physical or real addresses. Independent protection of address spaces is provided at each level. Information about the state of real memory pages is kept in segment registers or a segment register cache potentially enabling real memory access to occur simultaneously with address calculation, thereby increasing performance of the computer system.] A fast physical address is generated in parallel with a fully computed virtual-linear-physical address in a system using segmentation and optional paging. This fast physical address is used for a tentative or speculative memory reference, which reference can be canceled in the event the fast physical address does not match the fully computed address counterpart. In this manner, memory references can be accelerated in a computer system by avoiding a conventional translation scheme requiring two separate and sequential address translation operations – i.e. from virtual to linear, and from linear to physical .

IN THE CLAIMS

Please cancel claims 1 – 5.

Please amend claim 38:

38. A system for performing address translations, [said system generating an actual physical address from a virtual address in a time period T, by calculating a linear address based on said virtual address, and by calculating said actual physical address based on said calculated linear address, said system further including] comprising:

means for generating an actual physical address from a virtual address in a time period T, by calculating a linear address based on said virtual address, and by calculating said actual physical address based on said calculated linear address; and

a fast physical address generator for generating a fast physical address related to said virtual address in a time < T.

Please add the following claims (82 – 112):

82. A system for performing memory references in a processor which employs both segmentation and optional paging during an address translation, said system comprising:

means for performing an address translation by generating a first physical address from a first virtual address by first calculating a first linear address based on a first segment identifier and first offset associated with the first virtual address, and then calculating the first physical address based on the first calculated linear address; and

a fast physical memory access circuit for generating a fast memory reference, which fast memory reference is based on physical address information from said address translation means;

a bus interface circuit for initiating a fast memory access to a memory subsystem based on said fast memory reference.

83. The system of claim 82, further including a comparator for determining whether said fast memory reference can be used for a fast memory access.

84. The system of claim 83, further including a cancellation circuit for canceling said fast memory access.

85. The system of claim 84, wherein the system performs an actual memory reference after said fast memory reference is cancelled.

86. A method for performing memory accesses between a processor and a memory, said processor having virtual addresses that are segmented and optionally paged, the method comprising the steps of:

generating computed physical addresses by converting virtual addresses having a segment identifier and a segment offset into linear addresses, and then converting said linear addresses into a physical addresses;

generating a speculative physical address based on one of said computed physical addresses;

initiating a speculative memory access based on said speculative physical address.

87. The method of claim 86, further including a step of initiating an actual memory access based on a physical address which has been computed during separate segmentation and paging operations.

88. The method of claim 87, wherein said speculative memory access is completed unless canceled in favor of an actual memory access.

89. A system for performing a first and a second address translation of first and second virtual addresses respectively, the system comprising:

a virtual to linear address converter circuit generating a first calculated linear address based on the first virtual address; and

a linear to physical address converter circuit completing the first address translation by generating a first calculated physical address from said first calculated linear address, said first calculated physical address including a first calculated page frame and a first calculated page offset; and

wherein the system uses information from the first address translation during the second address translation so that the second address translation can be performed in less time than the first address translation.

90. The system of claim 89, further including a comparator for determining whether said second address translation can be used for a memory access.

91. The system of claim 89, wherein said second address translation is based on a combination of partial linear address information relating to said second virtual address and physical address information from a different virtual address.

92. The system of claim 89, wherein the system also calculates an actual second physical address from said second virtual address, by calculating a second linear address based on a second segment identifier and second offset associated with said second virtual address, and calculating said second physical address based on said second calculated linear address.

93. The system of claim 92, wherein at least a portion of said actual second physical address is compared with a corresponding portion of said second physical address from said fast physical address generator, and when said portions are not equal, said actual second physical address is used for a memory access.

94. The system of claim 89, further including a register for storing address information pertaining to the first virtual address for use during said translation of said second virtual address.

95. A circuit for performing fast translations of virtual addresses to physical addresses in a computer system, the circuit including:

an address generator performing a first address translation of a first virtual address having an associated first segment identifier and a first offset;

said address generator also performing a fast address translation of a second virtual address having an associated second segment identifier and a second offset;

wherein said address generator uses information from the first address translation during the fast address translation so that said translation of said second virtual address takes less time than said first address translation.

96. The system of claim 95, further including a comparator for determining whether said fast address translation can be used for a memory access.

97. The system of claim 95, wherein said fast address translation is achieved based on a combination of partial linear address information relating to said second virtual address and physical address information from said first virtual address.

98. The system of claim 95, wherein the address generator also performs a calculated translation to calculate an actual second physical address from said second virtual address, by calculating a second linear address based on said second segment identifier and second offset associated with said second virtual address, and calculating said second physical address based on said second calculated linear address.

99. The system of claim 98, wherein at least a portion of said actual second physical address is compared with a corresponding portion of said second physical address from said fast physical address generator, and when such portions are not equal, said actual second physical address is used for a memory access.

100. The system of claim 95, further including a register for storing address information pertaining to the first virtual address for use during said translation of said second virtual address.

101. A method of translating virtual addresses in a computer system, the method including the steps of:

(a) generating a first calculated physical address based on a first virtual address in a first operation, said first virtual address including a first segment identifier and a first offset; and

(b) generating a second fast physical address in a second operation based on a second virtual address, said second virtual address including a second segment identifier and a second offset, and said second fast physical address being generated based on information obtained during said first operation;

wherein said second operation takes less time to perform in said computer system than said first operation.

102. The method of claim 101, further including a step of determining whether a memory access can be made using said second fast physical address.

103. The method of claim 101, wherein during step (b) said second physical address is generated based on a combination of partial linear address information relating to said second virtual address and physical address information from said first virtual address.

104. The method of claim 101, further including a step (c): generating an actual second physical address from said second virtual address during a third operation, by calculating a second linear address based on said second segment identifier and second offset associated with said second virtual address, and calculating said second physical address based on said second calculated linear address.

105. The method system of claim 104, further including step (d): comparing at least a portion of said actual second physical address with a corresponding portion of said second physical address from said fast physical address generator, and when such portions are not equal, using said actual second physical address for a memory access.

106. The system of claim 101, further including a step of storing address information pertaining to the first virtual address in a register during said first operation for use during said second operation.

107. A method of performing address translations in a computer system, the method including the steps of:

(a) performing a first address translation by translating a first virtual address into a first physical address by: (i) first calculating a first linear address based on a first segment identifier and first offset associated with said first virtual address; and (ii) calculating said first physical address based on said first calculated linear address and

(b) performing a second address translation using information obtained during said first address translation to translate a second virtual address into a second physical address; wherein said second translation can be achieved in less time than said first translation.

108. The method of claim 107, further including a step of determining whether a memory access can be made using said second physical address.

109. The method of claim 107, wherein during step (b) said second physical address is generated based on a combination of partial linear address information relating to said second virtual address and physical address information from said first virtual address.

110. The method of claim 107, further including a step (c): generating an actual second physical address from said second virtual address, by calculating a second linear address based on said second segment identifier and second offset associated with said second virtual address, and calculating said second physical address based on said second calculated linear address.

111. The method system of claim 110, further including step (d): comparing at least a portion of said actual second physical address with a corresponding portion of said second physical address from said fast physical address generator, and when such portions are not equal, using said actual second physical address for a memory access.

112. The system of claim 107, further including a step of storing address information pertaining to the first virtual address in a register for use during said second address translation.